Problem Report PR-002

HW part: HW0001

HW rev: R002

Description: PCB hardware is not able to assert CRESET to hold FPGA in reset.

Steps to recreate the problem:

1. Apply +5V to 5V input
2. Verify 1.2V appears at 1.2V rail
3. Verify 3.3V appears at 3.3V rail
4. Verify Mode LED illuminates with 50% duty cycle

Test result: Partial Pass

Resolution: Swap CRESET (IC1 pin 34) and CDONE (IC1 pin 35) signals so that CRESET is on an output (I/O) pin and CDONE is on an input (I) pin.